Notice of Allowability	Application No.	Applicant(s)	
	10/644,850	SHINOHARA, MAHITO	
	Examiner	Art Unit	
	Pritham Prabhakher	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/12/2007*.

2. ☒ The allowed claim(s) is/are *2-10 and 12-15*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date [redacted].

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Continuation of Attachment(s) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 03/24/2004 and 12/21/06.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jennifer Reda on 05/04/07.

The application has been amended as follows:

The following changes to the drawings have been approved by the examiner and agreed upon by applicant:

*In **Figure 7**, the following items have been re-numbered as follows*

1 to 101, 2 to *102, 3* to *103, 4* to *104, 5* to *105, 6* to *106, 7* to *107, 8* to *108, 9* to *109, 10* to *110, 11* to *111, 12* to *112 and 13* to *113.*

In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

Allowable Subject Matter

Claims 2-10 and 12-15 are allowed.

The following is an examiner's statement of reasons for allowance:

*In regard to independent **Claim 4**, the closest prior art fails to teach or reasonably suggest "an image pickup device comprising an array of a plurality of pixels including photoelectric conversion portions for accumulating signal charges generated by photoelectric conversion and an amplifying transistor for amplifying the signal charges generated by said photoelectric conversion portion to output the amplified signal charges, said device comprising: a junction-type field effect transistor comprising a main electrode made of a first semiconductor region of a first conduction type connected to a control electrode region of said amplifying transistor included in two pixels adjacent to each other, and a control electrode region made of a second semiconductor region of a second conduction type opposite to the first conductive type having the same electric potential as that of a semiconductor region of the second conduction type included in a semiconductor region forming said photoelectric conversion portions, said junction-type field effect transistors arranged in a same line connecting to each other in series;*

an electric potential supplying circuit for supplying predetermined electric potential to the main electrode region of said junction-type field effect transistor; and

***a potential control circuit for controlling electric potential of said firs semiconductor region by means of capacity coupling**".*

Regarding **Claims 2-3, 5-10 and 14**, these claims are allowed as being dependent from allowed independent claim 4.

*In regard to independent **Claim 12**, the closest prior art fails to teach or reasonably suggest "an image pickup device comprising an array of a plurality of pixels including photoelectric conversion portions for accumulating signal charges generated by photoelectric conversion, and an amplifying transistor for amplifying the signal changes generated by said photoelectric conversion portion to output the amplified signal charges, said device comprising:*

a junction-type field effect transistor comprising:

a first main electrode made of a first semiconductor region of a first conduction type connected to a control electrode region of said amplifying transistor;

a control electrode region made of a second semiconductor region of a second conduction type opposite to the first conductive type having the same electric potential as that of a semiconductor region of the second conduction type included in a semiconductor region forming said photoelectric conversion portions;

a second main electrode made of a third semiconductor region of a first conduction type connected to a potential supply portion for supplying a predetermined electric potential; and

***a potential control circuit for controlling electric potential of said first semiconductor region by means of capacity coupling**.*

Regarding **Claims 13 and 15**, these claims are allowed as being dependent from allowed independent claim 12.

The following are the closest references found:

Watanabe (US Patent No.: 6163023) *disclose an amplified photoelectric transducer of the present invention that includes: a photoelectric transducer section for photoelectrically transducing incident light into an electric signal; a first MOS transistor for amplifying the electric signal; a second MOS transistor for resetting the photoelectric transducer section; and a third MOS transistor for reading out to a signal line the amplified electric signal. The photoelectric transducer section includes a signal charge storage section for storing a charge corresponding to the electric signal and a potential change detection section for detecting a potential change of the electric signal. The amplified photoelectric transducer further includes a fourth MOS transistor for switching the potential of the potential change detection section to a semiconductor substrate potential in response to an operation of the third MOS transistor.*

Orava et al. (US Pub No.: 2001/0001562A1) *disclose an imaging device comprises a semiconductor substrate including an array of pixel cells. Each pixel cell comprising an individually addressable pixel circuit for accumulating charge resulting from radiation incident on a pixel detector. The pixel circuit and the pixel detector can either be implemented on a single substrate, or on two substrates bonded together. The charge storage device can be a transistor, for example one of a pair of FET transistors*

connected as a cascade amplification stage. An imaging plane can be made up of one imaging device or a plurality of imaging devices tiled to form a mosaic. The imaging devices may be configured as a slot for certain applications, the slit or slot being scanned over the imaging plane. Control electronics can include addressing logic for addressing individual pixel circuits for reading accumulated charge from the pixel circuits. Imaging optimization can be achieved by determining maximum and minimum charge values for pixels for display, assigning extreme grey scale or color values to the maximum and minimum charge values and allocating grey scale or color values to an individual pixel according to a sliding scale between the extreme values. Scattered radiation can be detected and discarded by comparing the detected pixel value to a threshold value related to a minimum detected charge value expected for directly incident radiation and discarding detected pixel values less than said threshold value.

Nakamura et al. (US Patent No.: 6836291B1) *disclose a solid-state, two-dimensional image sensing device having a matrix of pixels each of which employs a photosensor that generates a photocurrent and a MOS circuit which outputs a signal proportional to the logarithm of the integral over time of the photocurrent. The sensor includes an integration control-switching device so that all pixels in the array have equal integration time. The sensor integrates the signal for each pixel for a period of time and stores the integrated signal in a pixel signal storage location. To read out the stored signal each pixel includes an amplifier to increase the signal during read out. The sensor further accumulates signal in either a MOS transistor pn-junction or a secondary pixel storage location during a time that the integrated pixel signal is being read out so*

that image information can be collected continuously even while the integrated pixel signal for each pixel is being read.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pritham Prabhakher whose telephone number is 571-270-1128. The examiner can normally be reached on M-F (7:30-5:00) Alt Friday's Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pritham David Prabhakher
Patent Examiner
Pritham.Prabhakher@uspto.gov

Pritham . D. Prabhakher

DAVID OMETZ
SUPERVISORY PATENT EXAMINER